MODUL 9 SIMULASI RANGKAIAN BCD-TO-7 SEGMENT

9.1 Tujuan Praktikum Modul 9

Setelah mempraktekkan topik ini, praktikan diharapkan dapat:

- 1. Praktikan dapat mengenal dan mengetahui BCD to 7 segment
- 2. Praktikan dapat membuat rangkaian BCD to 7 segment
- 3. Praktikan dapat mensimulasikan rangkaian BCD to 7 segment

9.2 Dasar Teori Praktikum Modul 9

9.2.1 7-Segment

Seven segment adalah suatu segmen – segmen yang digunakan untuk menampilkan angka/bilangan decimal. Seven segment ini terdiri dari 7 batang LED yang disusun membentuk angka 8 dengan menggunakan huruf a-g yang disebut DOT MATRIKS. Setiap segment ini terdiri dari 1 atau 2 LED (*Light Emitting Dioda*).





Seven-Segment Display

Seven segment dapat menampilkan angka – angka decimal dan beberapa karakter tertentu melalui kombinasi aktif atau tidaknya LED penyusunan dalam seven segment. Untuk mempermudah pengguna seven segment, umumnya digunakan sebuah decoder atau sebuah seven segment driver yang akan mengatur aktif atau tidaknya led-led dalam seven segment sesuai dengan inputan biner yang diberikan.

9.2.2 BCD to 7-Segment

Decoder BCD to Seven segment adalah decoder yang mengubah nilai biner BCD ke dalam tujuh bit data seven segment untuk ditampilkan nilai desimalnua secara visual Bagan Decoder BCD to seven segment dan tampilan display seven segment.



Gambar 9.2 Decoder BCD to 7 Segment

Tabel Kebenaran

Adapun data keluaran *Decoder BCD to Seven segment* ditunjukkan pada table dibawah ini:

DESIMAL	D	С	В	Α	a	b	с	d	e	f	00	7-LED
0	0	0	0	0	0	0	0	0	0	0	1	8
1	0	0	0	1	1	0	0	1	1	1	1	8
2	0	0	1	0	0	0	1	0	0	1	0	8
3	0	0	1	1	0	0	0	0	1	1	0	8
4	0	1	0	0	1	0	0	1	1	0	0	8
5	0	1	0	1	0	1	0	0	1	0	0	8
6	0	1	1	0	1	1	0	0	0	0	0	8
7	0	1	1	1	0	0	0	1	1	1	1	3
8	1	0	0	0	0	0	0	0	0	0	0	8
9	1	0	0	1	0	0	0	1	1	0	0	8
10	1	0	1	0	1	1	1	0	0	1	0	0
11	1	0	1	1	1	1	0	0	1	1	0	8
12	1	1	0	0	1	0	1	1	1	0	0	8
13	1	1	0	1	0	1	1	0	1	0	0	8
14	1	1	1	0	1	1	1	0	0	0	0	8
15	1	1	1	1	1	1	1	1	1	1	1	8

Tabel 9.1 BCD to 7 Segment Display Decoder

Setiap kombinasi nilai DCBA akan menampilkan simbol nilai desimal pada seven segment. Jika logika DCBA adalah '0000' maka seven segment akan menampilkan angka '0'. Jika nilai DCBA adalah '0001' maka seven segment akan menampilkan angka '1'. Dan seterusnya. Selengkapnya seven segment akan

menampilkan visual nilai. IC TTL *Decoder to seven segment* dimuat pada IC TTL 7447 dan 7448.

9.3 Lembar Kegiatan Praktikum Modul 9

9.3.1 Alat dan Bahan

- 1. Software Quartus 18.1
- 2. Laptop
- 3. Mouse

9.3.2 Langkah Praktikum Modul 9

1. Klik New Project Wizard



2. Klik Next

🕽 New P	roject Wizard	×
Intro	duction	
The Nev	v Project Wizard helps you create a new project and preliminary project settings, including the following:	
•	Project name and directory	
•	Name of the top-level design entity	
٠	Project files and libraries	
٠	Target device family and device	
٠	EDA tool settings	
You can menu). '	change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments You can use the various pages of the Settings dialog box to add functionality to the project.	
Don'	t show me this introduction again < Back	2

3. Kemudian tentukan Directory Project dan Nama Project, lalu klik Next

) New Project Wizard	
Directory, Name, Top-Level Entity	
What is the working directory for this project?	
C:\intelFPGA_lite\18.1\namamodul	
What is the name of this project?	
namamodul	
what is the name of the top-level design entity for this project? This name is case sensitive and must ex design file.	ictly match the entity name in the
namamodul	
< Back Next >	inish Cancel Help

4. Pilih **Empty Project**, kemudian klik **Next** lagi

Project Type elect the type of project to create. Pempty project Create new project by specifying project files and libraries, target device family and device, and EDA tool settings. Project template Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the Design Store.	
elect the type of project to create.) Empty project Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.) Project template Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, o download design templates from the <u>Design Store</u> .	
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5. Setelah itu klik **Next** lagi

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(×	Add All
ile Name	Type Libra	y Design Entry/Synthesis Tool	HDL Version		Remove
					Up
					Down
				P	roperties

 Lalu ganti Family ke MAX 10 (DA/DF/DC/SA/SF/SC), kemudian ketikkan di Nama Filter 10M50DAF484C7G, lalu klik Available Device yang tersedia, kemudian klik Next

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Device far	nily				Show in 'Available	devices' list			
Family:	MAX 10 (D	A/DF/DC/SA/SC)		•	Package:	Any		-	
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7. Kemudian klik **Next**

DA IOOIS.				
Tool Type	Tool Name	Format(s)		Run Tool Automatically
Design Entry/Synth	<none> 🔻</none>	<none></none>	*	Run this tool automatically to synthesize the current design
Simulation	<none> 👻</none>	<none></none>	~	Run gate-level simulation automatically after compilation
Board-Level	Timing	<none></none>	•	
	Symbol	<none></none>	+	
	Signal Integrity	<none></none>	•	
	Boundary Scan	<none></none>	W.	

8. Lalu klik **Finish**

New Project Wizard	
Summary	
When you click Finish, the project will be created with	h the following settings:
Project directory:	C:\intelFPGA_lite\18.1\modul 9
Project name:	modul9
Top-level design entity:	modul9
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	MAX 10 (DA/DF/DC/SA/SC)
Device:	10M50DAF484C7G
Board:	n/a
EDA tools:	
Design entry/synthesis:	<none> (<none>)</none></none>
Simulation:	<none> (<none>)</none></none>
Timing analysis:	0
Operating conditions:	
Core voltage:	1.2V
Junction temperature range:	0-85 °C
	< Book Newton Einich Concel Help

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9. Buat file baru dengan klik File, lalu New. Dapat juga menggunakan shortcut Ctrl+N.

File	Edit	View	Project	Assignments	Proce
	New			Ctrl+N	
Ta	Open			Ctrl+O	
	Close			Ctrl+F4	

10. Pilih Block Diagram/Schematic File, kemudian klik OK.



11. Cari komponen BCD to 7 Segment dengan cari "7447" pada Symbol Tool



12. Masukan 4 pin input pada project board



13. Sambungkan pin input pada komponen BCD to 7 Segment pada pin A, B, C, D



14. Pasang 7 pin output pada komponen BCD to 7 Segment



15. Compile hasil rangkaian dengan cara pilih compile design pada bagian task >> klik kanan → start >> yes → tunggu compiling hingga sukses



16. Lalu masuklah ke University Program VWF dengan CTRL+N

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	Veniog HDL File							
	VHDL File							
×	Memory Files							
	Hexadecimal (Intel-Format) File							
	Memory Initialization File							
~	Verification/Debugging Files							
	In-System Sources and Probes File							
	Logic Analyzer Interface File							
	Signal Tap Logic Analyzer File							
	University Program VWF							
~	Other Files							
	AHDL Include File							
	Block Symbol File							
	Chain Description File							
	Synopsys Design Constraints File							
	Text File	2						
		4						

17. Lalu akan muncul tampilan seperti ini

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	0 ps	5						

18. Lalu buka **Edit → Insert → Insert Node Bus → Node Finder → List** lalu klik tanda ('>>')

Named: *		Filter	Dingual	1			-	ok
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Look in: *						List	С	ancel
Nodes Found:			S	elected No	des:			
Name	Туре	^		Nam	e	1	Туре	1
in_ A	Input			_ A		Input		
в В	Input		>	🔓 В		Input		
in_ C	Input		>>	⊢ C		Input		
in_ D	Input			🔓 D		Input		
💾 qA	Output			at qA		Output		
out qB	Output		<< 0	📕 qB		Output		
out qC	Output		9	ut qC		Output		
out qD	Output		9	ut qD		Output		- 1
💾 qE	Output		9	💾 qE		Output		
out qF	Output	~	9	aF		Output		*

19. Masukan A : clock periode 10ns dan duty cycle 50%

Masukan B : clock periode 20ns dan duty cycle 50%

Masukan C : clock periode 40ns dan duty cycle 50%

Masukan D : clock periode 80ns dan duty cycle 50%



20. Akan muncul hasil seperti ini

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- 21. Lalu buka **Simulation** → **Run Timing Simulation**
- 22. Tunggu progress flow simulation selesai
- 23. Akan muncul seperti ini

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24. Klik pin planner

25. Lalu masukan pin seperti ini



26. Lakukan **Compile Design**, setelah selesai proses **Compile Design** maka langkah prakikum modul 8 Rangkaian Decoder telah selesai

9.4 Soal Jurnal

- 1. Apa yang dimaksud dengan BCD to 7 Segment?
- 2. Buatlah rangkaian BCD to 7 Segment seperti ini pada software Quartus!



3. Isilah keluaran 7 Segment pada table berikut!

Α	B	С	D	Keluaran 7 segment
0	1	0	1	
1	1	0	1	
1	1	1	1	
0	0	0	1	
0	0	1	1	
1	0	0	1	
0	1	1	0	
1	0	0	0	
1	0	1	1	

4. Tuliskan apa yang telah dilakukan pada praktikum modul 9 menggunakan Bahasa kalian sendiri!