MODUL 10 SIMULASI *COUNTER* DAN *REGISTER*

10.1 Tujuan Praktikum Modul 10 :

Setelah mempraktekkan topic ini, praktikan diharapkan dapat :

- 1. Mengetahui dan memahami konsep dasar dari rangkaian *counter* dan *register* serta dapat membedakan jenis-jenis pada counter dan register.
- 2. Dapat membuat rangkaian *counter* dan *register* pada quartus prime lite.

10.2 Dasar Teori Praktikum Modul 10

10.2.1 Register

Register merupakan rangkaian untuk menyimpan data per bit. Register tersusun dari rangkaian flip-flop yang digunakan untuk menyimpan data sementara sebelum data diolah lebih lanjut, register juga digunakan untuk pergerakan/transmisi data pada operasi computer. Salah satu implementasi register adalah shift register atau resgister penggeser. Rangkaian shift register berfungsi untuk menyimpan data sementara dan untuk pergeseran data ke kiri atau ke kanan. Shift register juga terdapat beberapa macam yaitu PIPO, SISO, SIPO, PISO.



Gambar 10.1 Pergeseran Data Pada Register Geser

Macam-macam tipe Shift Register :

1. Register Parallel In Parallel Out (PIPO)

Register parallel in parallel out (PIPO) merupakan register geser yang input dan outputnya parallel, register geser PIPO akan mengubah format nilai dari data yang digeser dengan format data tetap parallel. Contoh : IC TTL 74LS174





2. Register Serial In Serial Out (SISO)

Register serial in serial out (SISO) merupakan register yang input dan outputnya seri. Register SISO tidak mengubah format data, yang berubah adalah nilai dari data tersebut. Contoh : IC TTL 74LS91





3. Register Serial In Parallel Out (SIPO)

Register serial in parallel out (SIPO) merupakan register geser yang inputnya seri dan output parallel. Register ini akan menggeser data secara seri dan mengeluarkannya dalam format parallel tanpa mengubah nilai data tersebut. Contoh : IC TTL 74LS164

		pa dat	ralel a out	
		D1	D2	D3 D4
serial • data in	D O			
	-0-	-0-	-0-	<u> </u>
clock 🔶				

Gambar 10.4 Register Serial In Parallel Out (SIPO)

4. Register Parallel In Serial Out (PISO)

Register parallel in serial out (PISO) merupakan register geser yang inputnya parallel dan output seri. Register ini hanya mengubah format data parallel menjadi output serial tanpa mengubah nilai dari data tersebut.



Gambar 10.5 Register Parallel In Serial Out (PISO)

10.2.2 Counter

Counter berfungsi sebagai pencacah bit, digunakan untuk menghitung banyaknya pulsa yang dimasukan pada suatu rangkaian digital.

Jenis-jenis counter :

1. Counter Up

Counter up dapat menghitung secara berurutan dari bilangan terkecil sampai bilangan terbesar atau bisa juga disebut sebagai penghitung maju. Up Counter dibagi menjadi 2 :

a. Synchronous Up

Synchronous up merupakan penghitung maju dimana setiap flip-flopnya menerima input secara bersamaan karena counter sinkron dirangkai secara parallel.

Gambar 10.6 Synchronous Up Counter



b. Asynchronous Up

Asynchronous up merupakan penghitung maju dimana flip-flop dirangkai secara seri sehingga flip-flopnya menerima clock dari sumber yang berbeda, keluaran tiap flip-flop digunakan sebagai clock untup flip-flop berikutnya secara berurutan.

Gambar 10.7 Asynchronous Up Counter



2. Counter Down

Counter down dapat menghitung dari nilai yang sudah ditentukan ke nilai terkecil atau bisa disebut sebagai penghitung mundur. Down Counter dibagi menjadi 2 :

1. Synchronous Down

Synchronous down merupakan penghitung mundur dimana setiap flipflopnya menerima input secara bersamaan karena counter sinkron dirangkai secara parallel.





2. Asynchronous Down

Asynchronous down merupakan penghitung mundur dimana flip-flop dirangkai secara seri sehingga flip-flopnya menerima clock dari sumber yang berbeda, keluaran tiap flip-flop digunakan sebagai clock untup flip-flop berikutnya secara berurutan.



Gambar 10.9 Asynchronous Down Counter

3. Counter Up dan Down

Counter up dan down merupakan rangkaian yang menggunakan perhitungan maju dan mundur.

10.3 Lembar Kegiatan Praktikum Modul 10 :

10.3.1 Alat dan Bahan

- 1. Mouse
- 2. Laptop
- 3. Quartus Prime Lite

10.3.2 Langkah Praktikum Modul 10

1. Buka software quartus prime lite, lalu klik New Project Wizard.



2. Klik Next

Introduction The New Project Ward helps you create a new project and preliminary project settings, including the following: Project Tame and directory Name of the top-level design entity Project Tales and libraries Target device family and device EDA tool settings Vou can charge the settings for an existing project and specify additional project-wide settings with the Settings command (Assignment menu). You can use the various pages of the Settings dialog box to add functionality to the project.	Introduction The New Project Wizard helps you create a new project and preliminary project settings, including the following: Project files and lifectory Read of the top-level design entity The Project files and lifectorie Target device family and device EDA tool settings You can use the various pages of the Settings dialog box to add functionality to the project. Don't show me this introduction again Don't show me this introduction again	
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3. Kemudian tentukan Directory Project dan Nama Project, lalu klik Next.

New Project Wizard					×
Directory, Name, Top-Level Entity					
What is the working directory for this project?					
C:\intelFPGA_lite\18.1\prakmod11					
What is the name of this project?					
prakmod11					
What is the name of the top-level design entity for this project? This design file.	name is case se	ensitive and mu	st exactly match	n the entity nam	e in the
prakmod11					
Use Existing Project Settings					
	< Back	Next >	Finish	Cancel	Help

4. Pilih Empty Project, kemudian klik Next lagi

New Project Winned	
New Project Wizard	
Project Type	
Select the type of project to create.	
Empty project	
Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.	
) Project template	
Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime download design templates from the <u>Design Store</u> .	oftware, or
< Back Next > Finish Cancel	Help

5. Setelah itu, klik Next lagi

ote: you can always add design	files to the project later.	
e name:		Add
k		X Add All
ile Name Type Library Desig	gn Entry/Synthesis Tool HDL Version	Remove
		Up
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		Properties

6. Ganti family ke MAX 10 (DA/DF/DC/SA/SF/SC), kemudian ketik nama filter 10M50DAF484C7G, lalu klik available device yang tersedia, terakhir klik Next.

New Project Wizard							
Family, Device &	& Board Setting	s					
Device Board	_						
Celest the family and	l device very weet to the	ant for com	nilation				
You can install additi	ional device support wi	th the Instal	l Devices comr	nand on the Tools m	ienu.		
To determine the ver	sion of the Quartus Pri	me software	in which your	target device is supp	ported, refer to the	e Device Support List	webpage.
Device family				Show in 'Available	devices' list		
Family: MAX 10 (DA/DF/DC/SA/SC)		•	Package:	Any		•
Device: All			•	Pin count:	Any		•
Target device				Core speed grade:	Any		•
O Auto device sel	ected by the Fitter			Name filter:	10M50DAF4840	27G	
Specific device	selected in 'Available d	evices' list		Show advanced	devices		
Other: n/a							
Available devices:							
Name	Core Voltage	LEs	Total I/Os	GPIOs	Memory Bits	Embedded multi	plier 9-b
10M50DAF484C7G	1.2V	49760	360	360 16	577312	288	
<							>
				< Back Nex	t > Finish	n Cancel	Help

7. Klik Next

Dol Name Format(s) Run Tool Automatically Design Entry/Synth Run Tool Automatically Disign Entry/Synth Run this tool automatically to synthesize the current design Simulation Run gate-level simulation automatically after compilation Board-Level Timing Symbol Signal Integrity Boundary Scan					
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		Boundary Scan	<none></none>	7	

8. Setelah itu klik **Finish.**

Summary	
Vhen you click Finish, the project will be created with	n the following settings:
Project directory:	D:\dotexe\app\intelFPGA_lite\18.1\namamodul
Project name:	namamodul
op-level design entity:	namamodul
lumber of files added:	0
lumber of user libraries added:	0
Device assignments:	
Design template:	n/a
Family name:	MAX 10 (DA/DF/DC/SA/SC)
Device:	10M50DAF484C7G
Board:	n/a
DA tools:	
Design entry/synthesis:	<none> (<none>)</none></none>
Simulation:	<none> (<none>)</none></none>
Timing analysis:	0
Operating conditions:	
Core voltage:	1.2V
Junction temperature range:	0-85 °C

9. Akan muncul tampilan seperti gambar di dibawah ini.

ectNavigator) — Hierarchy = u_a = • ompilation Hierarchy	IP Catalog Device Family Cyclone IV
ompilation Hierarchy	Device Family Cyclone N
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	V a Installed IP
	* Project Directory
	Y Library
	> Basic Functions
	> DSP
	> Interface Protocol
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10. Kemudian buat file baru dengan cara klik **File**, kemudian pilih **Block Diagram/Schematic**, lalu klik **OK**

0	New			×
	New Quartus F	Prime Project		^
~	Design Files			
	AHDL File			
	Block Diag	ram/Schemati	ic File	
	EDIF File			
	Qsys Syste	em File		
	State Mach	nine File		
	SystemVe	rilog HDL File		
	Tcl Script I	File		
	Verilog HD	L File		
	VHDL File			
×	Memory Files			
	Hexadecim	nal (Intel-Form	at) File	
	Memory In	itialization File	2	
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	In-System	Sources and F	Probes File	
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	Signal Tap	Logic Analyze	er File	~
	ОК	Cancel	Help	
	ОК	Cancel	Help	

11. Setelah workspace muncul, tulislah LPM COUNTER pada searching di sebelah kanan, lalu klik LPM_COUNTER, lalu akan muncul save IP variation, pilih tempat penyimpanan, kemudian klik VHDL, lalu OK.



Akan muncul gambar seperti di bawah ini, ubah bits menjadi 26, moduls menjadi 50000000, dan centang .bsf. Ikuti seluruh gambar di bawah.

	nouro		
no	🔨 MegaWizard Plug-In Manag	er [page 2 of 5]	? ×
•	🍓 LPM_COU	NTER	<u>About</u> <u>D</u> ocumentation
-	1 Parameter 2 EDA 3	Summary	
	General Ceneral 2	Optional Inputs	
	COUNTER clockmodulus %000000 q(25.0)	Which type of counter do you want? Plain binary Modulus, with a count modulus of 5000000 Do you want any optional additional ports? Clock Enable C Count Enable C C Count Enable C C C	arry-in arry-out
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Ì	MegaWizard Plug-In Manag	er [page 5 of 5]	? ×
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	MegaWizard Plug-In Manag LPM_COUI Parameter COUNTER COUNTER	er [page 5 of 5] SUTTER Summary Turn on the files you wish to generate. A gray checkmark in generated, and a green checkmark indicates an optional file The MegaWizard Plug-In Manager creates the selected files C: (Users \ASUS (Vusic)LAB MICRO) File COUNTER.vhc Variation file COUNTER.inc AHDL include file COUNTER.inc AHDL include file COUNTER.inc COUNTER.inc AHDL include file AHDL inc	? X About Documentation dicates a file that is automatically c. Click Finish to generate the selected files. giverard Pluy-Tim Manager sessions. is in the following directory:

13. klik kanan pada Workspace, kemudian klik Insert lalu Symbol.



14. Klik **Project**, klik counter yang telah dibuat, lalu klik **OK**.



15. Masukkan komponen-komponen (74393M, AND, NOT) dengan cara klik kanan lalu **Insert**, **Symbol** dan tulis nama komponen yang dicari.



16. Sambungkan komponen-komponen dengan **Orthogonal Node Tool**, dan gunakan **Orthogonal Bus Tool** untuk garis yang tebal, pasangkan juga output dan input seperti gambar di bawah.





17. Ubah orthogonal bus dengan cara klik kanan lalu **Properties**. Untuk orthogonal bus pada counter tuliskan "**q**[**25..0**]", sedangkan pada 74393M tuliskan "**q**[**25**]".



 Ganti nama output menjadi LED0-LED7 dan input menjadi CLKIN. Lalu klik Analysis & Synthesis. Setelah berhasil tanpa error maka praktikum modul 10 telah selesai.



10.4 Soal Jurnal

- 1. Jelaskan apa yang dimaksud dengan register dan counter! Menurut pemahaman kalian sendiri.
- 2. Jelaskan perbedaan asynvhronous dan synchronous counter!
- 3. Jelaskan perbedaan PIPO, SISO, SIPO, PISO dan contoh-contohnya!
- 4. Tuliskan apa yang telah dilakukan pada praktikum modul 10 menggunakan Bahasa kalian sendiri!